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ALU Using Area Optimized Vedic Multiplier

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ABSTRACT—The load on general processor is increasing. For Fast Operations it is an extreme importance in Arithmetic Unit. The performance of Arithmetic Unit depends greatly on it multipliers. So, researchers are continuous searching for new approaches and hardware to implement arithmetic operation in huge efficient way in the terms of speed and area. Vedic Mathematics is the old system of mathematics which has a different technique of calculations based on total 16 Sutras. Proposed work has discussion of the quality of Urdhva Triyakbhyam Vedic approach for multiplication which uses different way than actual process of multiplication itself. It allows parallel generation of elements of products also eliminates undesired multiplication steps with zeros and mapped to higher level of bit using Karatsuba technique with processors, the compatibility to various data types. It is been observed that lot of delay is required by the conventional adders which are needed to have the partial products so in the work it is further optimized the Vedic multiplier type Urdhva Triyakbhyam by replacing the traditional adder with Carry save Adder to have more Delay Optimization. The proposed work shows improvement of speed as compare with the traditional designs. After the proposal discussion of the Vedic multiplier in the paper, It is been used for the implementation of Arithmetic unit using proposed efficient Vedic Multiplier it is not only useful for the improve efficiency the arithmetic module of ALU but also it is useful in the area of digital signal processing. The RTL entry of proposed Arithmetic unit done in VHDL it is synthesized and simulated with Xilinx ISE EDA tool. At the last the proposed Arithmetic Unit is validated on a FPGA device Vertex-IV.

Keywords— Urdhva Triyakbhyam Sutra, Vedic mathematics, Carry Save Adder, VHDL

I. INTRODUCTION

As known that it is the era of digital domain where the digital signals and its processing is an important concern. The performance of DSP is greatly depends on the MAC unit. So by improving the MAC unit we can develop efficient the Digital Signal Processor, for that proposed Arithmetic unit appears very useful. Also modern CPUs are increasingly working on fast speed with reduced in size of transistor. Arithmetic and Logic Unit (ALU) is a most important and required blocks in CPU. So it is must to have fast and efficient ALU. ALU is the unit in Microprocessor or Microcontroller and execution unit to perform Arithmetic operations like Addition, Multiplication, Subtraction, and Division and also logical operations. In India, Vedic Mathematics is popular and which is heard lot of times so with as per this reference the methods for resolving computations mentally. One of the major purposes of Vedic mathematics is to execute the difficult calculations in simple manner, even orally manageable without much use of pen and paper. Any single human can do these mental operations for very small numbers and So Vedic mathematics gives approaches to solve operations with higher value numbers easily. Vedic mathematics contains more than one method for every basic arithmetic operation like multiplication and division.For every operation there is at least one defined method provided along with some generic methods which are directed towards particular cases simplifying the calculations further. [6], [7] described the Vedic mathematics from beginning and discuss all operations. Vedic mathematics provides algorithms to easy the mathematics and that makes it perfect solution for the problems with speed. Proposed work has used the Urdhva Triyakbhyam sutra for multiplication. Designing done with the Carry Save Adder (CSA) instead of the Conventional Adder which is required during the Partial Product generation with as known CSA converts the multi-operand addition into the easy two operand Addition and so the it requires less time.

II. PROPOSED ARITHMETIC UNIT

Proposed 32x32 bit Arithmetic Unit is given in the figure 1.

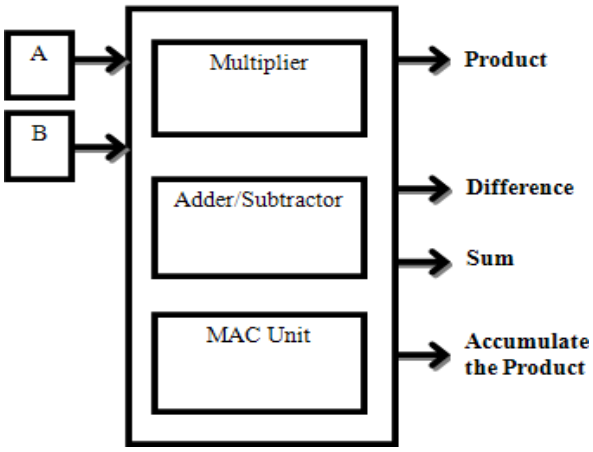

Fig 1.Arithmetic Module

Here the A and B are the two 32 bit inputs of proposed Arithmetic Unit. And other part of the design includes Adder, Subtractor, Multiplier, and MAC (optional when DSP processor in use). Product and Accumulated product are 64 bit output while differences, S are 32 bit output. Proposed work did not focus on the designing of the adder and subtractor circuits as these are not consider modules which consumes large amount of area and power in ALU. But after lots of study it is been found that generally, carry ripple adders can be used when it required to meet timing constraints because they are easy to build and compact. When word lengths of 32, tree adders are somewhat faster. Smart EDA synthesis tools automatically understand the "+" operator and map it on an appropriate adder to meet desired timing constraints keeping minimizing the area. The subtractor not different and can be designed with adder circuitry along with two's complement algorithm. [8] Has used the Vedic method for the design of multiplier. For designing sub module 'Multiplier' proposed work have also used the Vedic technique of multiplication named Urdhva Triyambakam multiplier though addition part of it with carry CSA. Urdhva Triyakbhyam method is a general multiplication formula useful to all cases of multiplication. It actual means Vertical and Cross wise. An example of multiplication using Urdhva Triyakbhyam approach is shown in following figure 2

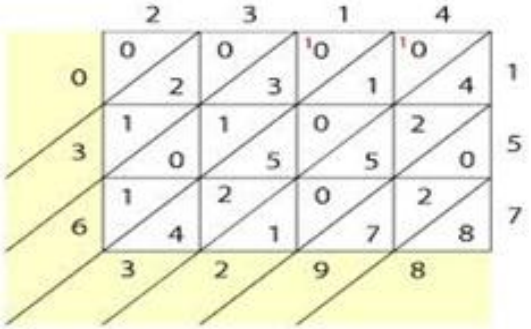

Fig 2. Vedic Multiplication on Decimal Numbers

Now discuss hardware design part of Vedic Multiplier. The design begins first with Multiplier design that is 2 bit multiplier as shown in figure 3.

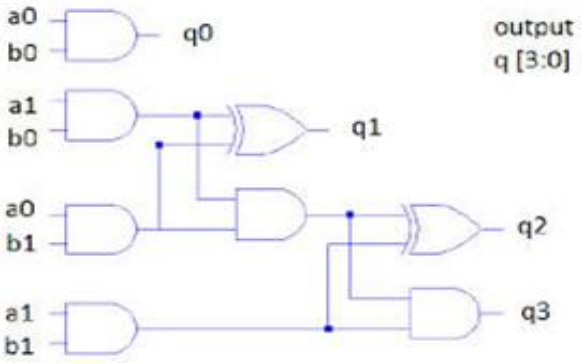

Fig 3. 2X2 Bit Multiplier

For 32x32 Multiplier, first the basic module, that the 2x2 bit multipliers have been design and then, with using these 2x2 blocks, 4x4 module has been design by adding the partial products using CSA and then using this 4x4 module, 8x8 bit module and then 16x16 bit module and then in last 32x32 bit Multiplier module. The block diagram using the Vedic algorithm for multiplication named Urdhva Triyambakam multiplier with carry CSA is given in the following.

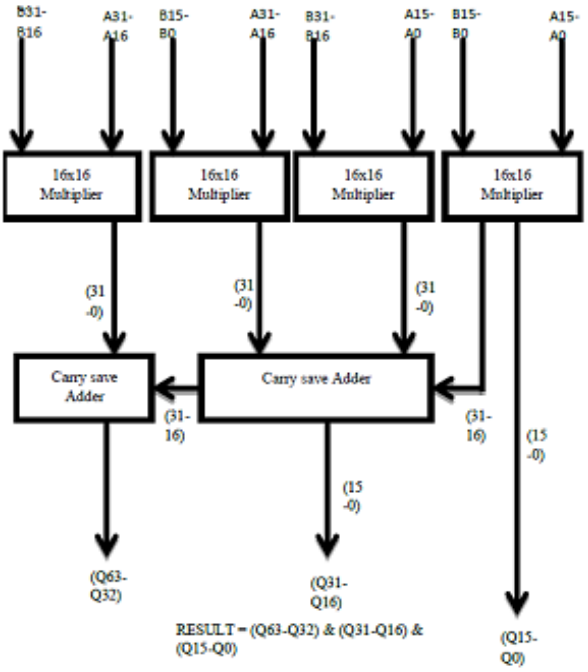

Fig.4 32 Bit
Multiplier with Carry save Adder

The MAC unit should be able to produce output in one clock cycle and the new result of addition is added to the previous one and stored in the accumulator register. Figure 4 given above shows MAC architecture which is used by us to design the Arithmetic Unit.

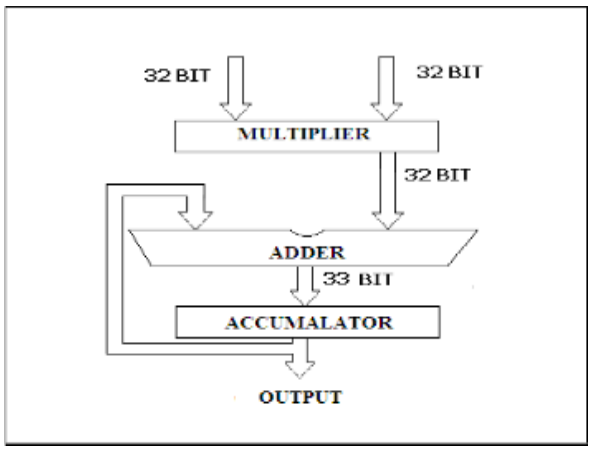

Fig 5. MAC Unit

III. RESULTS

Till now we have successfully design 4 bit vedic multiplier with the help of CSA and table given below shows the results for the same. Next 8x8 , 16x16 and 32x32 need to be implement. The results are been produced after RTL entry in Xilinx EDA tool. Simulation is done on Xilinx ISE and results are been verified correctly.

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No of Slices	19
No of 4 input LUT	33
No of bounded IOBs	16
Logical Delay	7.947 ns

Table 1 synthesize Results of 4 bit Proposed Vedic Multiplier

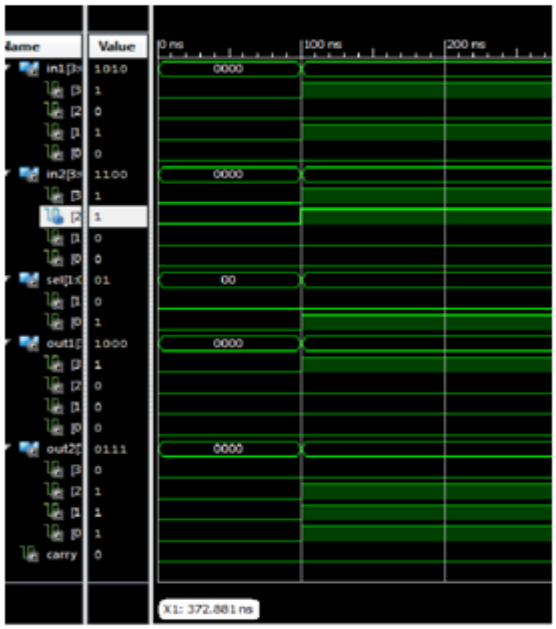

Figure 6: simulation of proposed 4 bit Vedic multiplier

IV. CONCLUSION

Proposed work have designed the 4x4 bit Multiplier which provides better results with respect to the available vedic multiplier or other Multiplier and as known dynamic power is proportional to the frequency (clock speed capacity) consumed to perform any operation. So, it can say that proposed design also reduces the dynamic power indirectly. This makes efficient multiplier and very useful for designing the delay and power optimized ALU, which can provide direct affect on the Microprocessor & microprocessor and also CPU whose performance is dependent on the efficiency of ALU. Proposed design can also be used for optimizing the MAC unit of DSP. And so the optimized designs can be made for FFT, FIR, IIR, and DFT whose performance is dependent on the speed of MAC unit.

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